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Issues in Current-Voltage/Capacitance-Voltage Traces-Based MIS Characterisation that Improves Understanding for a Better Design of n-channel MOSFETs on Si and SiC

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Abstract: *An n-MOS device in accumulation and an n-channel MOSFET in inversion behave like a Metal-Insulator-Metal device with a high concentration of electrons of the order of $10^{19}/cm^3$near the surface. The conduction band barrier height with the oxide conduction band remains the same for both the devices when the experimental threshold voltage of the MOSFET nullifies the effect of quantization of the ground state energy level of 0.2 eV where most of the electrons reside. There is a limitation imposed for the design of a high mobility n-channel MOSFETs on simple and compound semiconductors such as Si, SiC and GaN. Reducing NITs near the CB increases leakage current and lowers oxide breakdown strength by increasing the FN tunnelling current. The switching states (NITs) convert to fixed states (fixed oxide charges) due to either processing with O, N, H or by forming gate stacks such as SiO_2/Al_2O_3. The fixed charges are positive charges for the p-substrate MOS that increases the cathode field for electron tunnelling in the n-channel MOSFET, thereby increasing the current and lowering the breakdown field. The fixed charges are negative charges for the n-substrate MOS that increases the anode field for hole tunnelling in the p-channel MOSFET, thereby increasing the current and lowering the breakdown field. The electromagnetic radiation present in the ambient conditions may be sufficient to charge the NITs and lower the low field oxide current to less than 10^{-8} A/cm^2.*
Keywords*: Cathode, Metal-Oxide-Semiconductor, Quantum Confinement, Silicon, Silicon Carbide*

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I. Introduction

The present article is a sequel to the previous article [1]. Some significant issues in I-V/C-V based MIS characterisation have come upfront which have been discussed in this article. This leads to better understanding, for the design of n-channel MOSFETs on simple and compound semiconductors like Si, SiC and GaN. In the author's previous study [1], two interrelations between I-V and C-V traces were brought out. The first was that the slope of the high field Fowler-Nordheim (FN) tunnelling current gets modified by the oxide voltage. The oxide voltage is corrected for the charges in the oxide and the metal-semiconductor work function difference and these charges are obtained from the high frequency C-V curve by determining the flat band voltage which is a measure of these charges [2]. The second interrelation was that the low field leakage current in the oxide is lowered with the charging of the NITs present in the oxide near the CB. The capacitance of the NITs can be obtained with the help of low frequency quasi-static C-V ramp rate of 0.1V/s, by dividing the observed low field gate leakage current in the n-MOS device in accumulation or a p-MOS device in inversion by the ramp rate. The average density of NITs can then be obtained from the capacitance by dividing the capacitance by (qA(kT)). A study by Simmons and Wei [3] had evolved a similar formula for direct determination of interface trap density at the Fermi level of a MOS device in non-equilibrium (depletion) by using the concept of the product of current and time being proportional to the trap density. This formula is developed as equation (31) in their article [3].

The author has been studying the MOS device for more than 30 years now and has been able to reveal some new applied science concepts which are built around four principles of Physics namely: conservation of charge, electromagnetism as explained by Maxwell's equations, quantum mechanics, Fowler Nordheim (FN) tunnelling of electrons and holes. A hole is actually the absence of a valence electron bonded to the bonding site of a material such as Si or SiC. So essentially, one can just say, FN tunnelling of electrons. William Watson and Benjamin Franklin in 1746 and 1747 independently proclaimed conservation of charge. But, the first convincing proof of the concept was given by Michael Faraday in 1843. Maxwell's four equations came in 1865, with the first equation being the Gauss's Law that was published in 1813. The Gauss's Law is also based on conservation of charge which was proven by Faraday in 1843. In the fourth equation, Maxwell introduced the concept of displacement current across a capacitor with the changing electric field. This was added to the Ampere Circuital Law. Field emission was observed by many during the period of 1897 to 1928 with J.J.

Thomson winning the Nobel in 1906 for the discovery of electron as negative charges emitted from the cathode of the cathode ray tube due to field emission in 1897. The Nobel for determining the value of the electron charge as 1.602 x 10^{-19} Coulomb went to Robert A. Millikan in1909. It took about 28 years to actually arrive at the correct value with many Scientists/Professors working independently to determine its value [4]. The Table I below compiled from the article by Morrow [4] gives a quick chronological order of the determination of electric charge value.

Table I. How the value of electronic charge e was determined over 28 years.

Scientist/Professor	Value of electronic charge, e (esu)
James Clerk Maxwell, 1873	Proposed 'molecule of electricity'
G.J. Stoney, 1881, called it 'electrons'	3 x 10^{-11}
J.J. Thomson (Nobel) discovered electron experimentally as a negatively charge particle using cathode ray tube, and the value for e/m in 1897.	
J.S. Townsend (Thomson's graduate student), 1897-98	3 x 10^{-10}
J.J. Thomson, modified Townsend's value, 1898	6.5 x 10^{-10}
J.J.Thomson (repeated), 1902-03	3.4 x 10^{-10}
H.A. Wilson , 1903	3.1 x 10^{-10}
Planck, 1900	4.69 x 10^{-10}
Rutherford and Geiger, 1908	4.65 x 10^{-10}
Millikan and Begeman, preliminary value	4.06 x 10^{-10}
R.A. Millikan (Nobel) – Fletcher oil drop experiment, 1909	Within 0.1% of the current accepted value of 4.80 x 10^{-10}

Fowler and Nordheim gave the equation of tunnelling in 1928 [5], which in the present time has developed into the equation for the metal-oxide-semiconductor (MOS) device as [6, 7]:

$$J = AE_{ox}^{\ 2} \exp(-\frac{B}{E_{ox}})$$

where, J is the current density in A/cm^2, A is a constant in A/V^2, E_{ox} is the oxide electric field in MV/cm, and B is the slope constant in MV/cm. The slope constant B, can be determined from the $\Delta \ln (J/E_{ox}^2)/\Delta (1/E_{ox})$ plot called the 'FN plot'. The low frequency quasi-static C-V plot in the MOS device is the application of the displacement current C (dV/dt), found in Maxwell's fourth equation, and the use of Gauss's Law to determine the correct oxide field by adding or subtracting charges in the oxide and the metal-semiconductor work function difference is its application in the MOS device based on conservation of charge. Quantum confinement of electron in a rigid infinite potential well is applied to the triangular potential well at the surface of an n-channel MOSFET in inversion. Here, the Schrodinger's time-independent wave equation is solved for finding quantized energy states and wave functions as solutions to the equation. It is thus seen that the four principles of Physics in the author's studies have applications in the MIS characterisation, particularly with the insulator as thermal silicon dioxide (SiO_2) [8, 9].

II. Quantum confinement of electrons in the potential well of an n-channel MOSFET

A. Solving the Schrodinger's Equation

In classical systems, a particle is fully described by its position and momentum. In quantum mechanics, a system is described by its wave function, which contains the probabilities of possible positions and momenta. The Schrodinger equation is a linear partial differential equation that describes the wave function of a quantum-mechanical system. The time-dependent Schrodinger equation is given as:

$$\left(-\frac{\hbar^2}{2m}\nabla^2 + V \right)\psi = i\hbar\frac{\partial\psi}{\partial t} \qquad (1).$$

This equation is a partial differential equation in four variables, the three position coordinates of the particle x, y, z, and the time t. In the case where the potential energy V is independent of time and depends only on position, the wave equation represents standing waves. If ψ represents standing waves, then time must represent as a separate factor, i.e., if V is independent of time, the position and time coordinates are separate in equation (1), and so ψ may be expressed in the form:

$$\Psi = \phi(x, y, z)\, u(t) \qquad (2);$$

Where ϕ (x, y, z) is independent of time t and u(t) is independent of position. Substituting the value of ψ from (2) in equation (1), gives:

$$\left[-\frac{\hbar^2}{2m}\nabla^2 + V(x,y,z) \right]\phi(x,y,z)u(t) = i\hbar\frac{\partial}{\partial t}\{\phi(x,y,z)u(t)\}.$$

Dividing throughout by ϕ(x, y, z) u(t), gives:

$$\frac{1}{\phi(x,y,z)}\left[-\frac{\hbar^2}{2m}\nabla^2 + V(x,y,z)\right]\phi(x,y,z) = i\hbar\frac{1}{u(t)}\frac{\partial}{\partial t}u(t) \quad (3).$$

In the above equation, the left hand side is independent of time, while the right hand side is independent of the co-ordinates (x, y, z). So, if the above equation is to be satisfied, each side of (3) must be equal to a constant E, so that;

$$\frac{1}{\phi(x,y,z)}\left[-\frac{\hbar^2}{2m}\nabla^2 + V(x,y,z)\right]\phi(x,y,z) = E;$$

or $$\nabla^2\phi + \frac{2m}{\hbar^2}(E-V)\phi = 0 \quad \text{.....(4)}$$

and $$i\hbar\frac{1}{u(t)}\frac{\partial u(t)}{\partial t} = E \quad \text{.....(5)}$$

The time-independent Schrodinger's equation can be re-written in one dimension as:

$$E(\phi) = -\frac{\hbar^2}{2m}\frac{d^2\phi}{dx^2} + V(\phi) \quad \text{.....(6)}$$

The first term on the right is the kinetic energy and the second term is the potential energy. Considering a particle restricted to moving along the x-axis between x = 0 and x = L by ideally reflecting, infinitely high walls of a box as shown in Fig.1. Suppose the potential energy V of the particle is zero inside the box, but rises to infinity on the outside, that is,

V = 0 for $0 \le x \le L$
and V = ∞ for $x < 0$ and $x > L$.

In such a case, the particle is said to be moving in an infinitely deep potential well. The solutions to time-independent Schrodinger's equation (4) for the particular case of particle in an infinite well gives definite allowed values of E called eigenvalues and the corresponding wave function ψ called the eigenfunction where Φ in equation (4) is replaced by ψ.

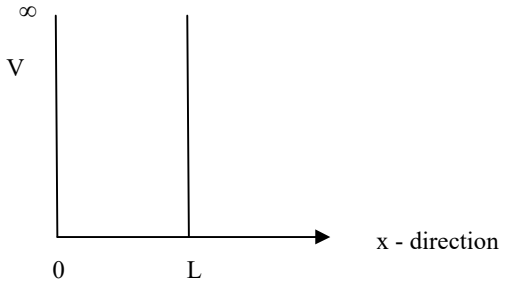

Fig.1.Particle in a rigid one-dimensional box of infinite potential well.

The Schrodinger's equation for the particle within the box (V = 0) is

$$\frac{d^2\psi}{dx^2} + \frac{2mE}{\hbar^2}\psi = 0 \quad (7)$$

If $\frac{2mE}{\hbar^2} = k^2$ is substituted in the above equation (4), then

$$\frac{d^2\psi}{dx^2} + k^2\psi = 0 \quad (8)$$

The general solution of this differential equation is of the form

$$\psi(x) = A\sin kx + B\cos kx \qquad (9)$$

where the constants A and B are determined by the boundary conditions. Since the particle cannot have infinite energy, it cannot exist outside the box. Therefore the wave function ψ must be zero outside the box. Ψ must also be zero at the walls, that is at x = 0, and x = L, for otherwise there would be discontinuities at the walls. The boundary condition ψ(x) = 0, at x = 0 applied to equation (6) makes B = 0. The condition ψ(x) = 0, at x = L makes A sin kL = 0. This means that kL = nπ, or k = nπ/L.
Writing E_n for E, and substituting for k^2 in equation (4) gives

$$E_n = \frac{n^2\pi^2\hbar^2}{2mL^2} \text{ for n = 1, 2, 3, ….} \qquad (10).$$

Thus, the particles in a potential well cannot have an arbitrary energy, but can take only certain discrete energy values corresponding to n = 1, 2, 3, …These are the 'eigenvalues' of the particle in the well and constitute the energy levels of the system. The integer n corresponding to the energy level E_n is called its 'quantum number'. Consider now, the eigenfunctions of the particle. Substituting B = 0 and k = nπ/L in equation (6), the allowed solution of the Schrodinger equation are

$$\psi_n(x) = A\sin\frac{n\pi x}{L} \qquad (11)$$

Using the normalization condition is $\int_{-\infty}^{+\infty}|\psi_n(x)|^2\,dx = 1$, the value of A can be found.

$$A^2\int_0^L \sin^2\frac{n\pi x}{L}\,dx = 1$$

This gives $A^2\left(\frac{L}{2}\right) = 1$ or $A = \sqrt{\frac{2}{L}}$. The normalized eigenfunctions of the particle are therefore;

$$\psi_n(x) = \sqrt{\frac{2}{L}}\sin\frac{n\pi x}{L} \qquad (12)$$

It can be seen that for n = 1, $\psi_1$is a half sine wave, and $\psi_1^2$is the probability density that informs about the position of the particle. It can be observed that the classical mechanics predicts the same probability for the particle anywhere in the box from equation (10), whereas, wave mechanics predicts that the probability is different at different points from square of the equation (12). To find the spacing between two adjacent energy levels for an electron moving in a box of size L, the difference in energies of two adjacent levels is given by:

$$\Delta E_n = E_{n+1} - E_n$$

Solving the above gives:

$$\Delta E_n = \frac{h^2(2n+1)}{8mL^2} \qquad (13)$$

Table II. Computed E_n and ΔEn values for n=1, between the adjacent energy level for an electron confined in an infinite potential well of length, L

Restricted Length for the particle to move, L (nm)	The first energy level, $E_1$from the bottom of the well, (eV)	Energy difference between the 1st and 2nd energy level, (3 x E_1), (eV)
0.1	38	114
1.0	0.38	1.14
1.5	0.169	0.509
2.0	0.095	0.286
2.5	0.061	0.183
3.0	0.042	0.127
5.0	0.015	0.0458
10.0	0.0038	0.0114
30.0	0.00042	0.00127
50.0	0.00015	0.000458

Sub-section II. A has been obtained from a condensed book on Quantum Mechanics by Satya Prakash [8], with the values of quantized energy states calculated by the author and tabulated as above. The author has reproduced the same value of 0.169 eV for L=1.5 nm from the formula developed by Stern [9] using equation

(13) from his formulation. His formulation is essentially the same for n-type inversion layers in Si, as that given above by Prakash in his book [8].

B. Quantization at the inverted Si surface of an n-channel Si MOSFET at the onset of strong inversion

An n-channel Si MOSFET fabricated on p<100> Si substrate having doping density of $10^{15}/cm^3$ is considered as an example. The inverted Si surface under the onset of strong inversion condition of surface potential ψ_s equal to bulk potential of $2\psi_B$ results in a thin inverted layer of electrons as the inversion capacitance, and a thick layer of depletion capacitance of about a 1000 nm. The inversion region of the MOSFET is a triangular potential well, where the electrons reside. It has been shown that the thin layer 2.5 nm of high surface density electrons of $10^{12}/cm^2$ to 1.5 nm of $10^{13}/cm^2$ exists at the strongly inverted region [10]. The depletion region density can be $10^{11}/cm^2$, giving the channel depth of $(10^{11}/10^{15}) = 10^{-4}$ cm, or 1000 nm. Considering the case of 1.5 nm of the strongly inverted region having an electron density of $10^{13}/cm^2$, it can be seen from the Table II above, that quantization results with the first energy level E_1 being 0.169 eV above the bottom of the conduction band at the Si surface. This energy value has been obtained by Stern in 1972 for the electron travelling perpendicular to the (100) surface based on the equation (3) of his research, that later on developed into equation (13) [9]. From this equation, the author calculated the E_0 value of 0.169 eV. Here, E_0 is same as E_1 presented in the Table II above. Weinberg further made a more accurate calculation in this value to 0.209eV at300 K [11]. This 0.2 eV energy level for the first energy state of the quantized well is where more than 70% of the electrons reside [12]. It lowers the Si/SiO_2 CBO from 3.2 eV to 3.0 eV (or 3.1 eV to 2.9 eV), and gives the value of the parabolic electron effective mass in SiO_2 as 0.50m [6]. This has been reviewed by Weinberg in his 1982 publication, for the FN tunnelling of electrons from the inverted Si substrate into the SiO_2 [6]. The author characterized the high field I-V characteristics of a polysilicon gated n-channel Si MOSFET of Eitan and Kolodny, and showed that by using the experimental threshold voltage and correcting the oxide voltage for polysilicon depletion potential at high fields, the parabolic electron and hole masses turnout to be 0.42m and 0.58m in thermal SiO_2[13]. The CBO and VBO for the Si/SiO_2 interface is calculated to be 3.2 eV and 4.6 eV, and the SiO_2 bandgap obtained is the accepted value of 8.9 eV, correct to the first decimal place [13]. The author has demonstrated recently in 2015 that the experimental threshold voltage is 0.4 V larger than the theoretical threshold voltage [14]. This 0.4V gate voltage translates into 0.2V of extra surface band bending practically [15, 16]. This extra band bending nullifies the decrease in the barrier height obtained by Weinberg. The barrier height therefore remains the same at 3.2 eV (or 3.1 eV) even after quantization of the energy states in the triangular potential well. So, simply put, quantization of the 1.5 nm thick inversion layer of electrons having high surface concentration of $10^{13}/cm^2$ exists, but the decrease in barrier height at the Si surface due to the first energy level being 0.2 eV above the bottom of the well is nullified if one considers the experimental threshold voltage that increases the depth of the well by an extra 0.2eV.

The concentration of electrons is calculated with the Si surface in accumulation and inversion. The concentration of electrons is given as [17]:

$$n = N_C \exp\left(-\frac{E_C - E_F}{kT}\right) \qquad (14).$$

Here, N_C is the density of states in the CB of the semiconductor Si or 4H-SiC, E_C is the bottom of the CB, E_F is the Fermi level of the doped semiconductor, Si or 4H-SiC, k is the Boltzmann constant and T is the temperature in Kelvin. In accumulation, E_c-E_F = 0, and so n= N_C which is about 2-3 x $10^{19}/cm^3$ at 300 K for both semiconductors. In inversion, the surface concentration is $10^{13}/cm^2$ for 1.5 nm thick inversion layer, giving the electron concentration as $(10^{13}/1.5 \times 10^{-7}) = 6.7 \times 10^{19}/cm^3$. Therefore, in both accumulation and inversion, the electron concentration is almost equal and high, and Si/SiO_2 FN tunnelling barrier height is the same at 3.2 eV, keeping in mind that in inversion, the experimental threshold voltage determined by extrapolating the current in the linear region, should be considered. The n-MOS device in accumulation and the p-MOS device in inversion as a n-channel MOSFET in the linear region [18, 19], behaves like an metal-insulator-metal (MIM) device with the metal-like semiconductor cathode and the metal anode with oxide as the dielectric between them and having the same barrier height with the CB of the oxide. The CBO for the SiO_2/Si is 3.2 eV and the CBO of the NO annealed SiO_2/4H-SiC (0001) Si-face is 2.78 eV. The above analysis indicates that these barrier heights do not change whether the device is in accumulation or inversion. The above analysis convinces the author as to why in the case of n-4H-SiC MOS device in accumulation, and the n-channel 4H-SiC MOSFET (on p-type epitaxial layer) in inversion, the density of border traps or near interface traps (NITs) are calculated to be the same at 300 K [1, 20]. For the n-type device in accumulation, the trap density is 23.5 x $10^{11}/cm^2eV$ at 300 K [1], and for the n-channel MOSFET in inversion in the linear region of conduction where there is strong inversion, the trap density of NITs is 26 x $10^{11}/cm^2eV$ at 300 K [20]. The samples of the n-type 4H-SiC MOS device studied in accumulation [1, 7] and the n-channel 4H-SiC MOSFET studied in inversion in the linear region have undergone similar oxide growth and NO annealing conditions with the author in the same collaborative experimental group [20]. Nitrogen at the interface is within 2 nm of the interface at the saturation level of about 2.5 x $10^{14}/cm^2$ giving a saturation concentration of N as 1.25 x $10^{19}/cm^3$ [21].

III. Designing of an n-channel 4H-SiC Power MOSFET

Near interface traps in the oxide (NITs) near CB of n-4H-SiC MOS device are present and their density is determined as 23.5 x 10^{11}/cm^{2}eV at 300 K and further extrapolated to lower temperatures up to 10 K.[1]. Reducing the NITs through processing with O, N or H, converts the switching states (NITs) to fixed states (fixed oxide charges). Positive charges appear in p-type MOS device and negative charges appear in n-type MOS device. In the n-type MOS device having negative charges with reduced NITs, the field at the cathode will reduce for electron tunnelling with the device in accumulation and breakdown field will therefore increase for electron conduction [2]. For the same n-type MOS device in inversion as a p-channel MOSFET, the anode field will increase for hole tunnelling causing larger current and therefore lowering the oxide breakdown field. Since there are reduced NITs, the surface mobility can be higher. In the p-type MOS device having positive charges with reduced NITs, the field at the anode will reduce for hole tunnelling with the device in accumulation and the breakdown field will therefore increase for hole conduction. For the same p-type MOS device in inversion as an n-channel MOSFET, the cathode field will increase for electron tunnelling causing larger current and therefore lowering the oxide breakdown field. Since there are reduced NITs, the surface mobility can be higher. For both, n-channel MOSFET on p-substrate and p-channel MOSFET on n-substrate, surface mobility can be higher due to reduced NITs through processing with O, N, and H, but the oxide breakdown will be lower due to switching states converting to fixed states as positive or negative charges.

The leakage current density in the devices with NITs will be less that 10^{-8} A/cm^2, and leakage current density without NITs will be exactly 10^{-8}A/cm^2, which is the displacement current of the oxide only [1]. The switching states are eliminated at the border, but the fixed states are created more inside the oxide. In our Vanderbilt 4H-SiC-MOS sample with NO annealing to saturation level [21], n-type MOS device has NITs near CB with the leakage current density less than 10^{-8}A/cm^2 (actually one order) in accumulation, and the p-type MOS device has positive charges with no NITs at the VB edge. The leakage current density is exactly 10^{-8} A/cm^2.in p-type MOS device in accumulation [1, 7]. This observation has been made by Kuhn in 1970 also, where he observed a current density of less than 10^{-8} A/cm^2 on n-Si-MOS device due to the presence of NITs [22]. The current density observed on wet oxidised C-face of n-type 4H-SiC was exactly 10^{-8} A/cm^2 because it did not have NITs but had a large density of negative fixed charges of 1 x 10^{12}/cm^2 due to excess of non-metals C and O [23]. These negative fixed charges in the oxide of n-type MOS device in accumulation reduces the field at the cathode for electron tunnelling but enhances the field at the anode for hole tunnelling in the inverted n-type MOS as a p-channel MOSFET. The current due to hole tunnelling increases and lowers the oxide breakdown field for the p-channel MOSFET

The switching states (NITs) will affect the surface effective and FE mobility due to Coulomb scattering [1]. As previously mentioned, reducing NITs means adding positive charges on p-type MOS device and adding negative charges on n-type MOS device. Thus a limitation is imposed. Reducing NITs to improve surface mobility will increase leakage current and lower oxide breakdown strength as switching states (NITs) convert to fixed states (fixed oxide charges).

Table III. Static relative dielectric constant, bandgap, CBO, and thermal conductivity of three commonly considered dielectrics for MIS devices.

Dielectric	Static relative dielectric constant	Bandgap, Eg, (eV)	CBO from Si/4H-SiC, (eV)	Thermal Conductivity, W/(cmK)
SiO_2	3.9	8.9	3.2/2.8	0.015
Al_2O_3	8	8.8	2.8/1.7	0.02
AlN	9	6	2.2/1.7	19

Consider further, the use of Al_2O_3 and AlN as a dielectric [24]. In particular, observe the CBO of the three dielectrics with Si in Table III above. The CBO of Si/SiO_2 is the largest at 3.2 eV on Si, and CBO of the 4H-SiC/SiO_2 is the largest at 2.8 eV on 4H-SiC. Also, among these two largest values, the CBO of the Si/SiO_2 is larger at 3.2 eV. Consider Al_2O_3 dielectric and n-channel 4H-SiC MOSFET. Al_2O_3 has a lower conduction band offset (CBO) with 4H-SiC than SiO_2. A lower CBO implies a lower slope constant B for the FN electron tunnelling in the n-MOS device in accumulation [2, 7]. A lower B means a higher exp(-B), and therefore a higher FN tunnelling current density J. A higher J for the same field E, is equivalent to lower E for the same J. Lower E for the same J means that there are negative charges in the n-MOS device in accumulation that lowers the cathode field for electron tunnelling and there are positive charges in the p-MOS device in accumulation that lowers the anode field for hole tunnelling. Negative charges for the n-MOS device in accumulation increases the anode field in the p-channel MOSFET for hole tunnelling thereby increasing the current and lowering the breakdown field. The positive charges in the p-MOS device in accumulation increases the cathode field in the n-channel MOSFET for electron tunnelling thereby increasing the current and lowering the breakdown field. So essentially, having a lower CBO for a different dielectric other than SiO_2 translates to having more positive charges in the oxide for n-channel MOSFET. Therefore, by using SiO_2/Al_2O_3 stack on 4H-SiC to make a n-

channel MOSFET means that there are more positive charges, although the mobility has increased due to lower total NITs from 1 nm SiO_2. That is, if one tries to improve mobility by reducing NITs, then more positive charges are equivalently added, which leads to increased leakage current and lower dielectric breakdown field due to higher tunnelling current as shown earlier. Once again, the same limitation is imposed. Reducing NITs to improve surface mobility increases leakage current and lowers oxide breakdown field as switching states (NITs) convert to fixed states (fixed oxide charges).

In general, the above analysis leads to the conclusion that increasing mobility in n-channel MOSFET by reducing NITs means, increasing positive charges that will increase the cathode field for electron tunnelling, thereby increasing the current and lowering the dielectric breakdown field, whether one uses gate stack or tries processing with O, N, H etc. with devices on the SAME semiconductor. The limitation applies to both Si and 4H-SiC n-channel MOSFETs. If one chooses a different semiconductor, such as 3C-SiC, which has a CBO with SiO_2 as 3.6 eV then, the situation becomes different. Here, the bandgap is smaller than 4H-SiC. It is 2.38eV. The NITs are in the CB and not inside the bandgap, so the mobility can be high. There is a high density of intrinsic defects [25] that can give a leaky oxide with low breakdown field, grown on it [26]. Good quality oxide can be grown by oxidation on a epitaxial 3C-SiC with less defects giving a displacement current density of the oxide capacitance only of 10^{-8} A/cm^2[27]. Here again it should be noted that the current density is exactly 10^{-8} A/cm^2 at low fields because there are no NITs on 3C-SiC devices [27]. The oxide breakdown is 8.5 MV/cm, and the effective mobility is 260cm^2/V-s [27]. However, because the bandgap is smaller than 4H-SiC, it has much larger concentration of intrinsic carriers which causes it to withstand lower fields. Therefore, it is limited to power MOSFET switch applications, where the off-state voltages are in the 400-600 V range [28].

IV. Voltage Ramp rates for the high frequency C-V curves at 1 MHz on MOS devices.

Study of the Fig.8 of the study by Winokur et al.[16] convinces the author of the choice of low frequency (LF) quasi-static ramp rate of 0.1V/s as the lower limit of the low frequency C-V trace from accumulation to inversion. It has been shown in Fig.8 of the reference that the high frequency (1 MHz) C-V curve obtained with voltage ramp rate from 100 V/s to 0.5V/s keeps the MOS device in the non-equilibrium 'deep-depletion' state when the minority carriers are not able to follow the ramp signal and are therefore not able to store charge and add capacitance to the depletion capacitance and cause inversion. At 0.1V/s, significant capacitance is added as the minority carriers are now following the ramp signal and causing inversion. Therefore, this 0.1 V/s is chosen to be the LF limit for the quasi-static C-V plot. This is the case for the p-type Si MOS device scanned from accumulation to inversion. In case of the wide bandgap 4H-SiC semiconductor, the minority carrier generation rate is so slow that inversion never happens at 300 K, unless the temperature is raised or ultra-violet (UV) radiation with energy greater than the bandgap of 4H-SiC (3.23 eV) is impinged upon the sample to generate minority carriers. However, if the minority carrier generation rate at 300 K would have been high, the p-type 4H-SiC MOS sample would also have shown inversion at the 0.1V/s ramp rate. With this premise, the use of 0.1V/s ramp rate for quasi-static LF C-V curve is justified. This ramp rate is equivalent to a low frequency of 0.32 Hz for a 50 mV ac signal. This is shown below. An ac signal is given and processed as:

$V=V_m$ Sin (wt)
$dV/dt = wV_m$Cos(wt)
Since the maximum value for Cos (wt)=1, therefore by taking V_m = 50 mV
$0.1=0.05 \times 2\pi \times f$
$f = (1/\pi) = 0.32$ Hz.

The high frequency of 1 MHz is chosen based on the emission rate of the occupied traps having a capture cross-section of 10^{-16}/cm^2 [29]. However, very high frequencies may be used up to 7-10 MHz to determine very fast interface states or trap densities of NITs in the oxide near CB of n-4H-SiC [30]. It has been shown by charge pumping experiments that the NITs in the oxide near CB of Si [31], as well as n-4H-SiC [1] are dominant at low frequencies of 1-100 Hz. A low frequency C-V characteristic on a p-type Si MOS device having SiO_2 as the gate dielectric shows a 'hump' in the capacitance as the capacitance in inversion is coming in parallel with the capacitance due to NITs and letting the total capacitance to rise causing a "hump"[32]. Hi-Lo C-V curve method is used to characterize the NIOTs in Si-based MOS devices [32]. The author has used the LF ramp rate of 0.1V/s (0.32 Hz) in his collaborative study by observing the low field leakage currents in MOS devices in accumulation and inversion to obtain total trap density of NITs [1, 7]. Subtracting the fast NITs [30] from the total NITs at 300 K [1, 20] results in 18×10^{11}/cm^{2}eV of 'not-so-fast-states'.

V. The electromagnetic radiation energies present in the solar spectrum

Observing the solar spectrum, photon wavelengths from 200 nm to 1400 nm are present that converts to energies of 1.24/0.2 to 1.24/1.4 eV based on E = (hc/λ) formula, where λ is the wavelength in μm.. This is equal to 6.2 eV to 0.9 eV. Therefore, it is easy to excite electrons from Si CB into the SiO_x CB. The Si/SiO_x CB offset is up to 3.2 eV for SiO_2. So electrons are getting trapped into NITs at 300 K due to photo-excitation at 300 K. There could be sub-3 nm SiO_x layer that contains border traps or even if there is a complete abrupt interface, the photo-excitation of electrons into SiO_2 can take place at 300 K to change the low voltage leakage current in the oxide. However, 2 nm thermal oxide has shown bulk property of SiO_2 such as the bandgap of 8.9 eV [33]. Even without applying any external voltage, the border traps are charged due to photo-excitation. Most of the time, the experiments in the laboratories are conducted under visible electromagnetic spectrum, which consists of wavelengths from 400 nm to 700 nm. The energy range for the radiation is 3.1 to 1.77 eV. This energy is also sufficient to charge NITs near CB of Si or 4H-SiC. A recent report by Afanasev has shown changes in the displacement current due to photo-conductivity with radiation energies less than the CBO energies in GaN-based MOS devices using SiO_2 or Al_2O_3 as dielectrics [34].

VI. Conclusion

It is concluded that an n-MOS device in accumulation and an n-channel MOSFET on p-substrate biased in the linear region behave like an MIM device with the semiconductor in the MOSFET having a high concentration of electrons ($10^{19}/cm^3$) in inversion of 1-2 nm thickness that gives the inversion capacitance. The n-MOS device in accumulation also has a high concentration of electrons ($10^{19}/cm^3$). For the n-channel Si MOSFET in inversion, the experimental threshold voltage is about 0.4 V larger that causes an extra band bending at the surface and nullifies the effect of quantization of the ground state energy level of 0.2 eV where most of the electrons reside. Thus, the CB barrier height with the oxide CB is kept the same as in accumulation, of 3.2 eV for example with Si. It is further concluded that there is a limitation imposed for the design of a high mobility n-channel 4H-SiC power MOSFET. While reduction of NITs in the oxide near the CB improves surface mobility, it increases leakage current and lowers oxide breakdown field. The switching states (NITs) convert to fixed states (fixed oxide charges) upon processing with O, N and H, or by using gate stack with 1 nm SiO_2/Al_2O_3. This limitation is also applicable to MOSFETs on other simple and compound semiconductors, such as Si and GaN. The electromagnetic radiation present in the ambient conditions may be sufficient to charge NITs near the semiconductor CB.

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